鸿芯科科技
Hxk Technology

LGS4200

Three-channel PMU :Buck and Boost converter with liner charger

Check for Samples: LGS4200

FEATURES

- Three-channel PMU:Buck,Boost and Super capacitor charger
- wide working range: 5V-40V
- 3.3V 450mA Output Power for Buck
- 12V 500mA Output Power for Boost at 2.7V Input
- 1% accuracy for Charger CV voltage and up to 150mA constant charge current
- High Efficiency PFM mode at light load for Buck
- Enable pin to auto-switch boost and charger
- Available in ES0P8 and QFN3x4-24 Package

APPLICATIONS

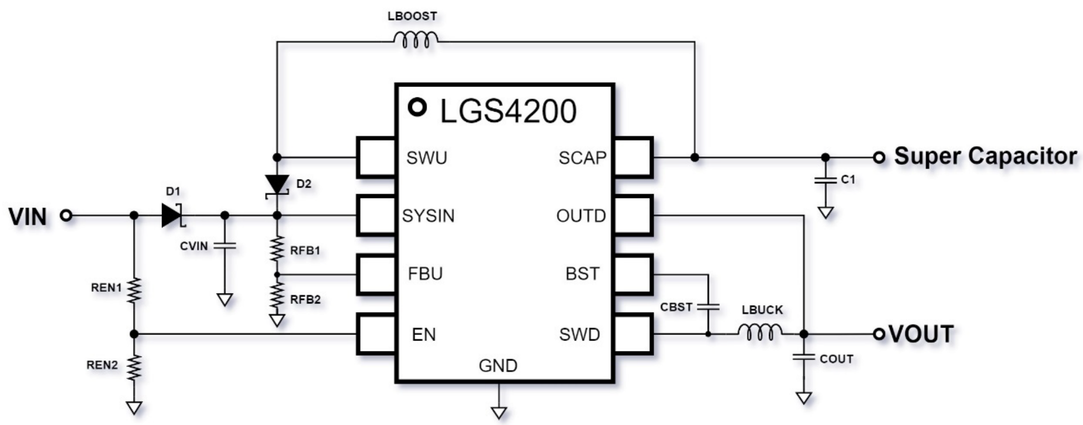
- PLC modules
- Power Meters
- Any system that needs super capacitor as a backup power

DESCRIPTION

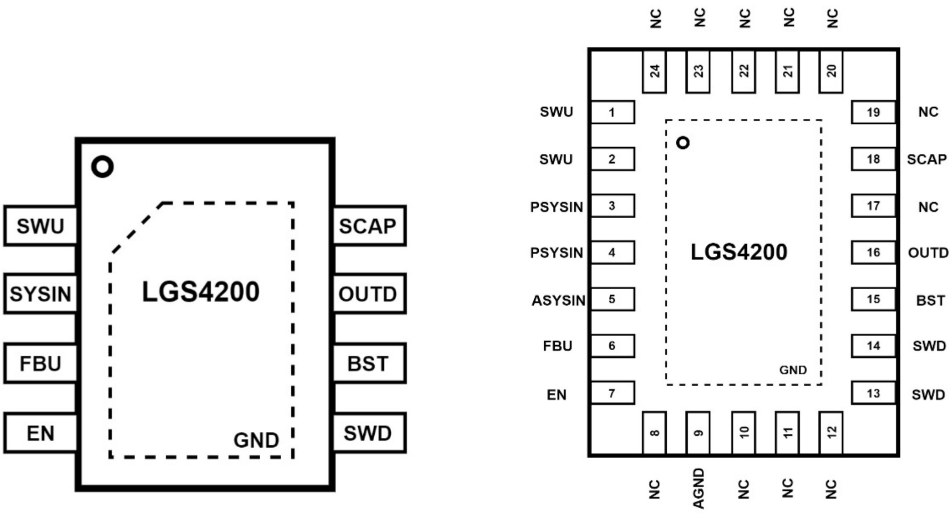
LGS4200 is a three-channel PMU that includes a 40V input, a high efficiency synchronous buck converter, a low startup, high efficiency 18V boost converter and a super capacitor Charger. The buck converter withstands input voltage up to 40V and delivers a 3.3V output with up to 450mA current. The boost converter is capable of providing up to 500mA to 12V output from a single cell super capacitor or a battery at 2.7V. A linear supercapacitor charger is also integrated with a very high accuracy CV voltage. The output voltage of boost can be adjusted by external resistor divider. All three power modules are packed into a single ES0P8 and QFN3x4-24 package, beating the discrete solution in features, performance, size, PCB layout and cost.

Part Number	Package
LGS4200	ESOP8 QFN3x4-24L

TYPICAL APPLICATION



Pin Configuration



ESOP-8 QFN3X4-24

Figure 5.1 PACKAGE REFERENCE TOP VIEW

Pin Functions

PIN NO.		NAME	DESCRIPTION
ESOP8	QFN3x4-24		
1	1,2	SWU	Switch PIN for BOOST
2	3,4,5	SYSIN	System Power Input PIN
3	6	FBU	External Feedback PIN for BOOST
4	7	EN	Enable PIN For Auto-switching BOOST (1)。
5	13,14	SWD	Switch PIN For BUCK
6	15	BST	Bootstrap PIN For BUCK. Connect a 10nF or bigger cap from BST to SWD
7	16	OUTD	Output PIN for BUCK, Fixed 3.3V. It is also the input of CHARGER
8	18	SCAP	Supercapacitor Output.It is internally programed to CV at 2.7V
9	9	GND	Power ground, Connect to system ground, and ground side of C_{VIN} and C_{OUT}
	8,10-12,17,19-24	NC	Not Connected

（1）EN=0,BOOST is ON, Charger is OFF; EN=1,BOOST is OFF, Charger is ON.

Absolute Maximum Ratings

Over operating free-air temperature range of -40°C to +125°C (unless otherwise noted)

参数	最小值	最大值	单位
SYSIN to GND	- 0.3	42	V
SWD,EN to GND	- 0.3+SYSIN	0.3+SYSIN	
SWU to GND	- 0.3	18	
BST to SWD	-0.3	6	
FB to GND	-0.3	6	
OUTD,SCAP to GND	-0.3	6	
储存温度（Storage temperature）T_{stg}	- 65	- 150	°C
结温（Junction Temperature）T_J	- 40	+ 125	

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

ESD Ratings

			VALUE	UNIT
V_{ESD}	Electrostatic discharge	Human-body model (HBM)	±2000	V
		Charged-device model (CDM)	±1000	V
		Machine Model (MM)	±200	V

Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

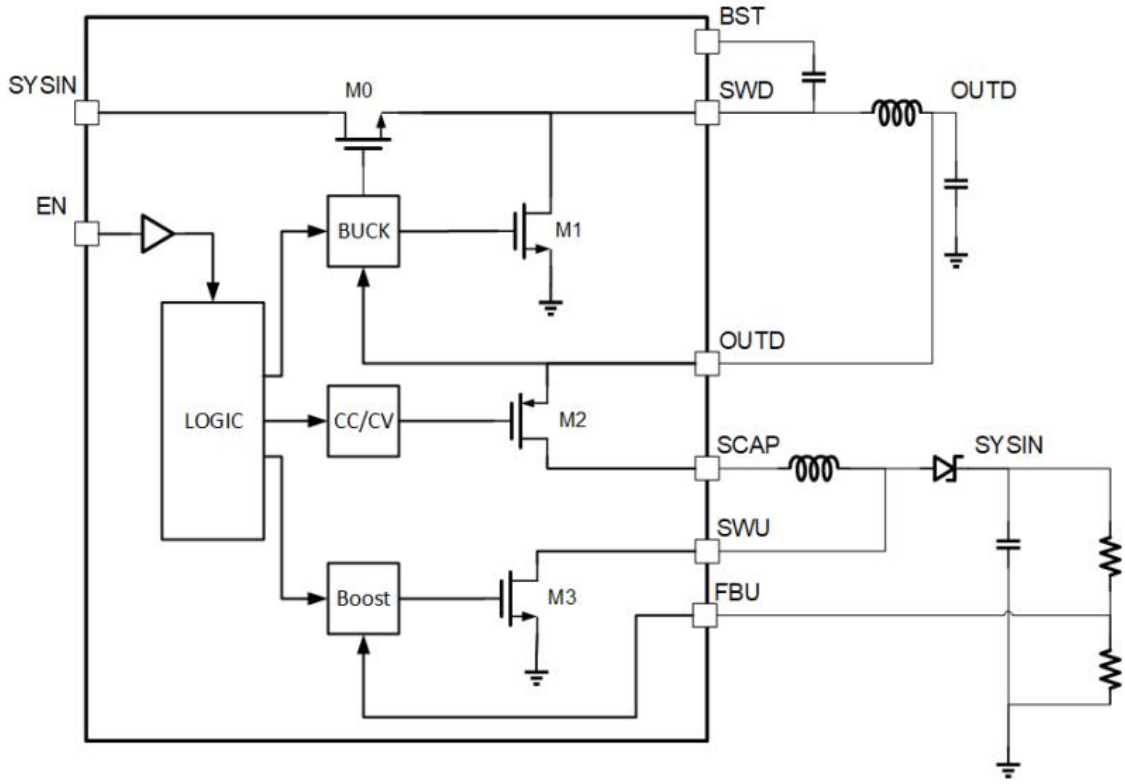
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits maybe more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

Electrical Characteristic

Limits apply over the recommended operating junction temperature (T_J) range of -40°C to +125°C, unless otherwise stated. Unless otherwise stated, the following conditions apply: VIN = 12 V, VOUT = 3.3 V

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
BUCK						
Input Voltage Range				4	40	V
Input Standoff Voltage				42		V
Input UVLO Rising				4.3		V
Input UVLO Falling				3.9		V
Input Over Voltage Projection				40		V
OUTD Voltage			3.2	3.3	3.4	V
Switching Frequency				830		KHz
Maximum Duty Cycle				95		%
High Side Switch On Resistance		I_{SWD}=100mA		360		mΩ
Low Side Switch On Resistance		I_{SWD}=100mA		300		mΩ
High Side Switch Current Limit				1.7		A
Low Side Zero Crossing Limit				50		mA
SWD Leakage Current		V_{SYSIN}=12V,V_{SWD}=0V,V_{OUTD}=3.5V		23		uA
BOOST						
Input Range			0.8		6	V
FBU Feedback Voltage			780	800	820	mV
FBU Input Current		V_{FBU}=0 V				nA
Output Voltage Range			3		18	V
Switching Frequency				1.1		MHz
Maximum Duty Cycle				88		%
NMOS Switch On Resistance				90		mΩ
NMOS Switch Current Limit				3.5		A
SWU Leakage Current		V_{SWU}=0 or 12 V,V_{EN}=0V			920	nA
CHARGER						
CV Voltage				2.7		V
Charge Current		Adjustable		50	150	mA
Dropout Voltage				360		mV
SYSTEM						
I_{SD}	Shut Down Current	EN=0,V_{FBU}=0.9V,V_{OUTD}=3.6V		79		µA
I_{CQ}	Shut Down Current Of Charger	V_{FBU}=0.9V,V_{OUTD}=3.6V,V_{SCAP}=3V		79		µA
EN Threshold		Rising，Hysteresis=65mV		1		V

Functional Block Diagram



Typical Applications

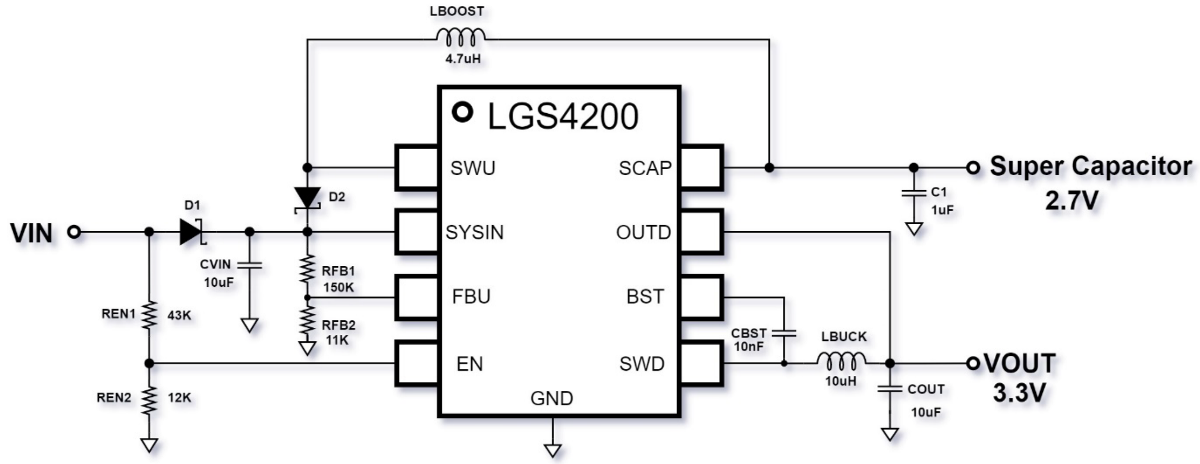
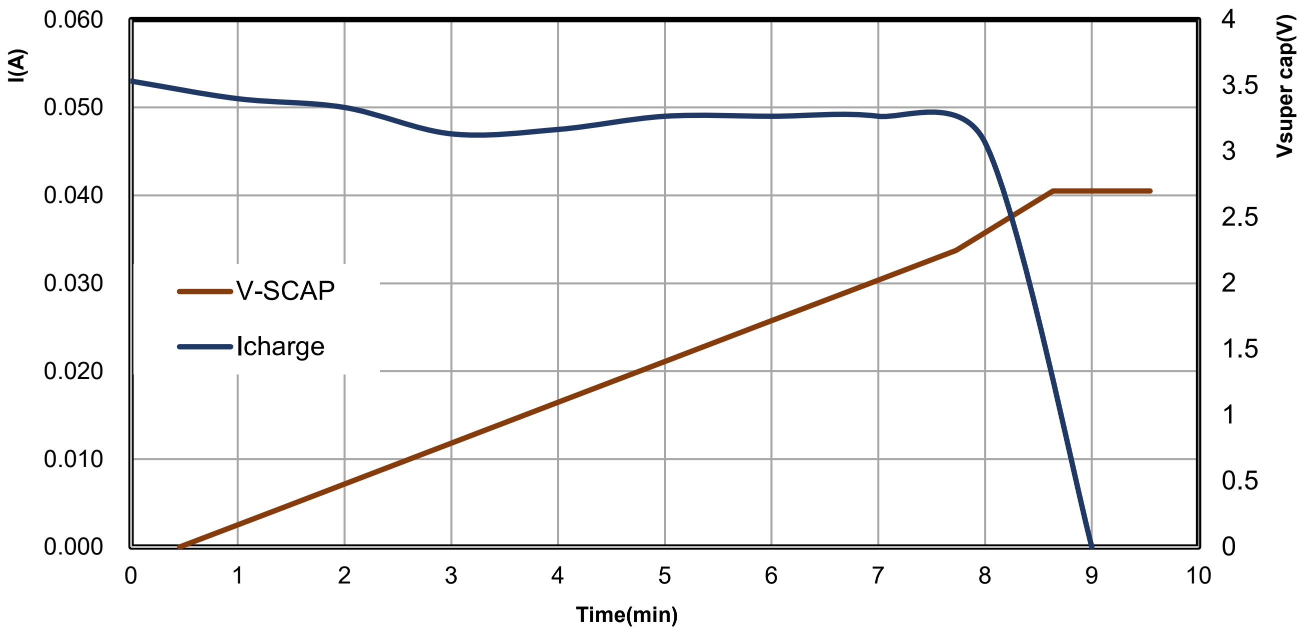


Figure 10. LGS4200 Basic Schematic

(1) It is recommended to use X7R or X5R ceramic capacitors as input capacitors, and place them as close to the IC as possible.

(2) For the capacitors from BST to SW, please choose ceramic capacitors with a withstand voltage higher than 10V, and place them as close to the IC pins as possible.

Charge Current and Voltage



Typical Characteristics

V_{SYSIN}=12V, V_{OUTD}=3.3V,L_{BUCK}=10uH,T_A=25°C unless otherwise note

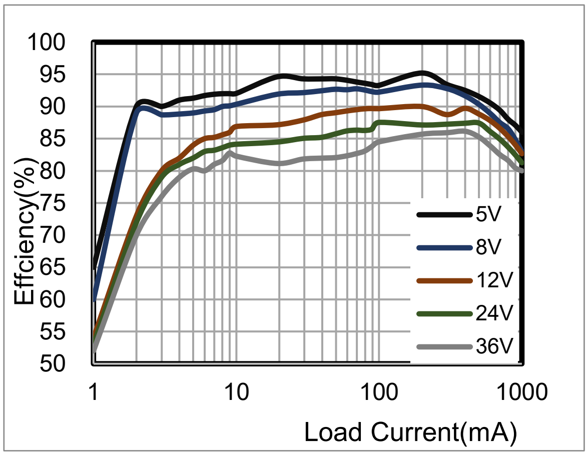


Figure11.1 Efficiency of BUCK

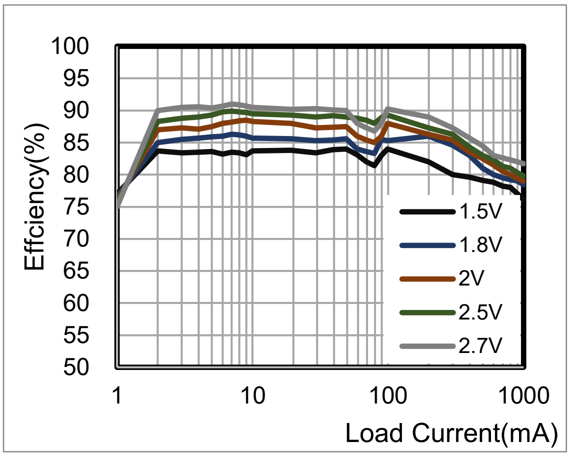


Figure11.2 Efficiency of BOOST

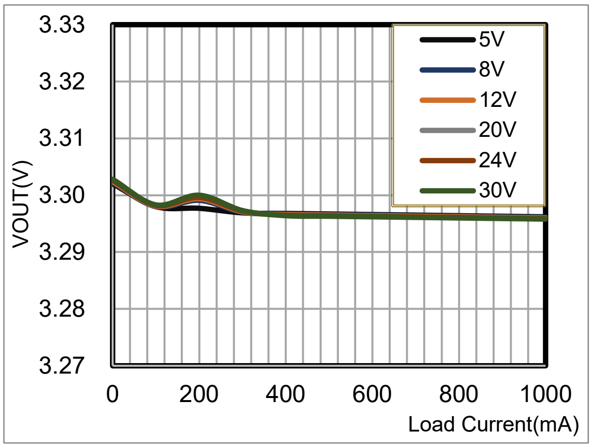


Figure11.3 Buck Load Regulation

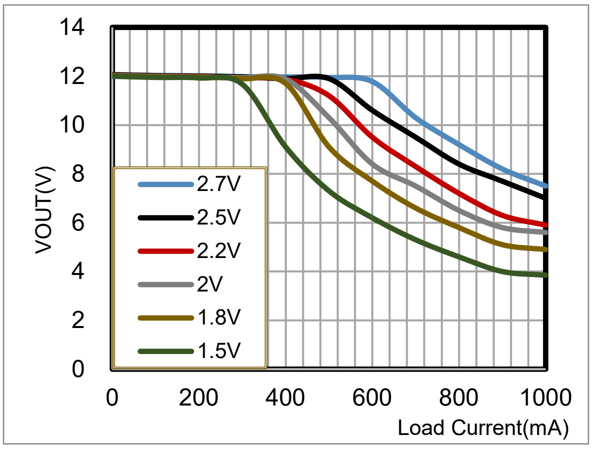
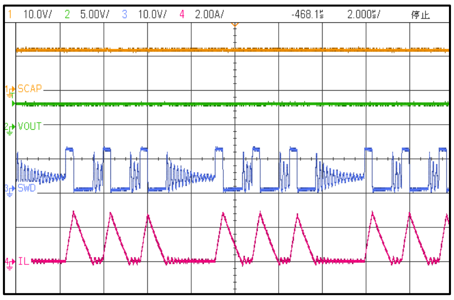
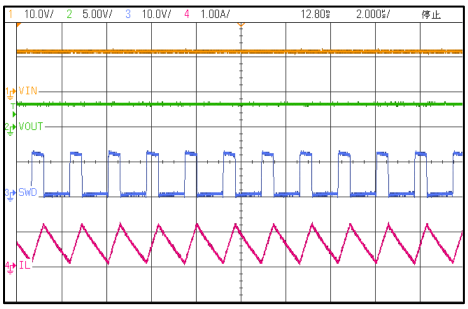


Figure11.4 Boost Load Regulation



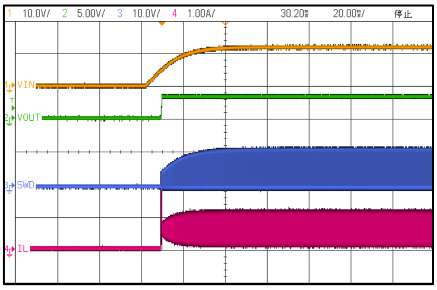
VIN=12V VOUT=3.3V LOAD=100mA

Figure11.5 Steady State DCM Of BUCK



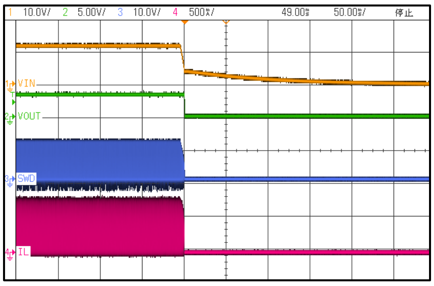
VIN=12V VOUT=3.3V LOAD=600mA

Figure11.6 Steady State CCM Of BUCK



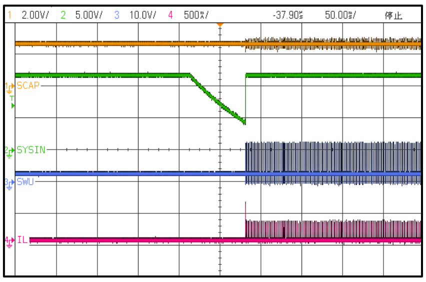
V_{IN}=12V V_{OUT}=3.3V CCM

Figure11.7 VIN Power On Of BUCK



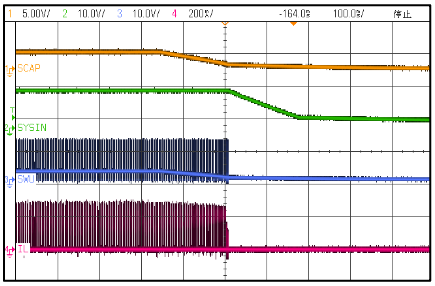
V_{IN}=12V V_{OUT}=3.3V CCM

Figure11.8 VIN Power Off Of BUCK



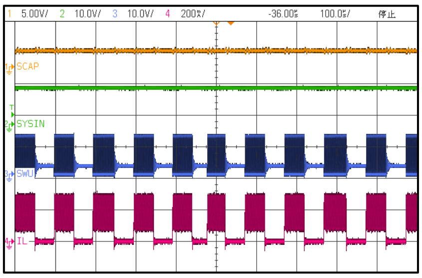
V_{IN}=2.7V V_{OUT}=12V

Figure11.9 VIN Power On Of BOOST



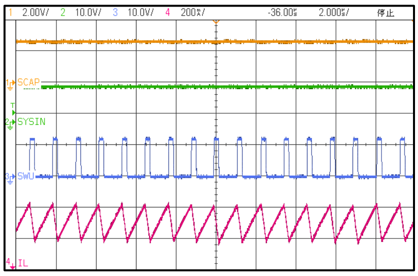
V_{IN}=2.7V V_{OUT}=12V

Figure11.10 VIN Power Off Of BOOST



V_{IN}=2.7V V_{OUT}=12V

Figure11.11 Steady State DCM Of BOOST



V_{IN}=2.7V V_{OUT}=12V

Figure11.12 Steady State DCM Of BOOST

Functional Description

Overview

The LGS4200 is a three-channel PMU that includes a wide input high efficiency synchronous buck converter, a low startup, high efficiency boost converter and a supercapacitor Charger. The buck converter withstands input voltage up to 40V and delivers a 3.3V output with up to 450mA current. The boost converter is capable of providing up to 500mA to 12V output from a single cell supercapacitor or a battery at 2.7V .A linear supercapacitor charger is also integrated with a very high accuracy CV voltage. The output voltage of boost can be adjusted by external resistor divider.

Buck converter

The BUCK has a wide input range, high-efficiency, synchronous step-down switching regulator which output is fixed at 3.3V; capable of delivering up to 0.45A of output current. With a fixed switching frequency of 800KHZ, this current mode PWM controlled converter allows the use of small external components, such as ceramic input and output caps, as well as small inductors. It also employs a proprietary control scheme that switches the device into a power save mode during light load, thereby extending the range of high efficiency operation. An OVP function protects the IC itself and its downstream system against input voltage surges With this OVP function, the IC can stand off input voltage as high as 40V.

Boost converter

The BOOST is a high efficiency no-synchronous step up converter. It is capable of delivering at least 6W of power from 2.7V, is 0.5A at 12V output. A switching frequency of 1MHz minimizes solution footprint by allowing the use of tiny and low-profile inductors and ceramic capacitors. The output of BOOST can beset by external resistor divider at FBU pin.

CHARGER

The CHARGER is fully integrated constant current (CC) / constant voltage (CV) function. It can deliver up to 150mA of charge current with a final float voltage of 1%.

Enable

EN is a digital control pin that turns the BOOST and CHARGER on and off. Drive EN High to turn on the CHARGER and turn off the BOOST, drive it Low to turn off the CHARGER and turn on the BOOST.

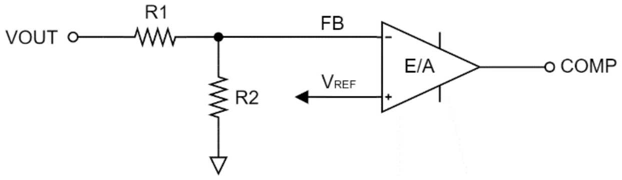
Over-Temperature Protection

Thermal protection disables BUCK, BOOST and CHARGER when the junction temperature rises to approximately 150°C; allowing the device to cool down. When the junction temperature cools to approximately 1350C; the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits regulator dissipation, protecting the device from damage as a result of overheating.

Application Information

BOOST Output Voltage Setting

The LGS4200 boost output is programmed using an external resistor divider. The output voltage is calculated using below equation.



$$R_2 = \frac{V_{FB}}{V_{OUT} - V_{FB}} \times R_1$$

A larger voltage divider resistor can reduce the current flowing through the voltage divider network and improve the voltage conversion efficiency. However, too large a resistance value will make the feedback loop more susceptible to noise. It is recommended to use a voltage divider resistor with an accuracy of ±1% or better, with a temperature coefficient of 100mmp or lower, and the resistance value of the resistor limited to K level. If the FB pin is grounded or disconnected, the output voltage value will be driven to near the input voltage value. It should be noted that the load connected to the output may be damaged at this time. The feedback loop should be kept away from PCB noise interference, please refer to the PCB layout reference given later.

BOOST-Charger Switching Voltage Setting

The LGS4200 EN pin also serves as a threshold voltage for auto-switching Super Capacitor Charger and the Boost. When the VIN drops and ENs voltage is below the falling threshold voltage (1V), the super-capacitor charger is disabled and the boost converter is then enabled at the same time. With a resistor ladder, R1 from VIN to EN and R2 from EN to GND; the VIN dropping threshold is programmed by the equation below.

$$R_2 = \frac{V_{EN}}{V_{SYSIN} - V_{EN}} \times R_1$$

R2 has to be between 1 k0hm to 20 K0hm.

Bootstrap capacitor C_{BST}

The LGS4200 buck driver high-side switch drive circuit requires a bias voltage higher than VDD to ensure that the high-side MOS tube is in the on state. The capacitor CBST between BST and SW acts as a "charge pump" to increase the voltage at the BST terminal to SW+VDD (V_{BST}-V_{SWD}=5V), and the conduction diode for charging CBST is integrated in the LGS4200 chip to minimize it as much as possible Use the size of the plan.
CBST recommends the use of 0.1μF capacitors with withstand voltage higher than 10~16V.

Input capacitance C_{VIN}

LGS4200 requires the use of decoupling capacitors to filter out noise interference at the input. The typical recommended value of the decoupling capacitor is 10μF, and the rated voltage must be greater than the maximum input voltage required by the IC, preferably twice the maximum input voltage. The increase of the capacitance can reduce the input voltage ripple and keep the input terminal voltage stable during load transients.

(1)The DC-Bias Effect of ceramic capacitors reduces the effective value of the capacitor. Please refer to the DC bias characteristics of the selected capacitor as much as possible to select the appropriate capacitor. Package size, rated voltage and dielectric material will cause the difference between the rated capacitance value and the effective capacitance value.

Output capacitance C_{OUTD}

LGS4200 allows the use of a wide range of output capacitor values. In order to ensure cost and small size, try to choose a suitable output capacitor. In practical applications, the output capacitor will directly affect the voltage overshoot/undershoot and the output voltage ripple during the transient response of the output current. When the load undergoes a transient change, the output capacitor needs to provide charge before the loop adjustment is completed. The transient voltage change value ΔV_{OUTD} can be calculated by the following formula:

$$\Delta V_{OUTD} = \Delta \mathrm{I}_{OUTD} * ESR$$

Where $\Delta \mathrm{I}_{OUTD}$ represents the jump value of the load current, and ESR is the equivalent series resistance of the output capacitor.

The output voltage ripple is composed of two parts: one is caused by the inductor current ripple flowing through the ESR of the output capacitor, and the other is caused by the inductor current ripple charging and discharging the output capacitor.

$$\Delta V_{OUTD-ripple} = \frac{\Delta I_L}{8 \times C_{OUTD} \times F_{SW}} + \Delta I_L \times ESR$$

ΔI_L represents inductor ripple current, F_{SW} represents MOSFET switching frequency.

In order to maintain a small output voltage overshoot or undershoot during transient changes and reduce output ripple, the capacitor needs to have a larger capacitance and a smaller ESR, which will also increase the cost and volume. Choose a suitable one The output capacitance is very important [1][2]。

(1) Excessive output capacitance will also affect the normal startup of the chip and loop stability.

(2) You can directly use the recommended 10μF, 100V, X7R ceramic capacitors in typical applications, or use it as a starting point for selecting the output capacitor value.

Power inductor L

The selection of power inductors mainly considers the saturation current of the inductor, which is based on the expected ripple current $I_{OUT-MAX}$ that is, the effective value of the AC current in the inductor that changes with the load current. Generally, it is controlled between 20%-40% of the maximum load current. The inductance value can be calculated by the following formula:

$$\Delta I_L = \frac{(V_{IN} - V_{OUT}) \times D}{L \times F_{SW}}$$

D represents the duty cycle of the switch, which can be approximated by $D = \frac{V_{OUT}}{V_{IN}}$ and the unit of the inductance value obtained is μH.

The inductor saturation current value must be higher than the sum of the maximum load current and ripple current:

$$I_{L-MAX} \geq I_{OUT-MAX} + \frac{\Delta I_L}{2}$$

Generally speaking, choosing an inductor with a lower inductance value will have a smaller DCR, which can cope with a faster transient response, and the size of the application scheme is smaller. However, an inductance that is too low will produce a larger inductor current ripple, resulting in a larger output voltage ripple when the same C_{OUTD} is used.

After testing, the recommended inductance value in typical applications can be used as a reference

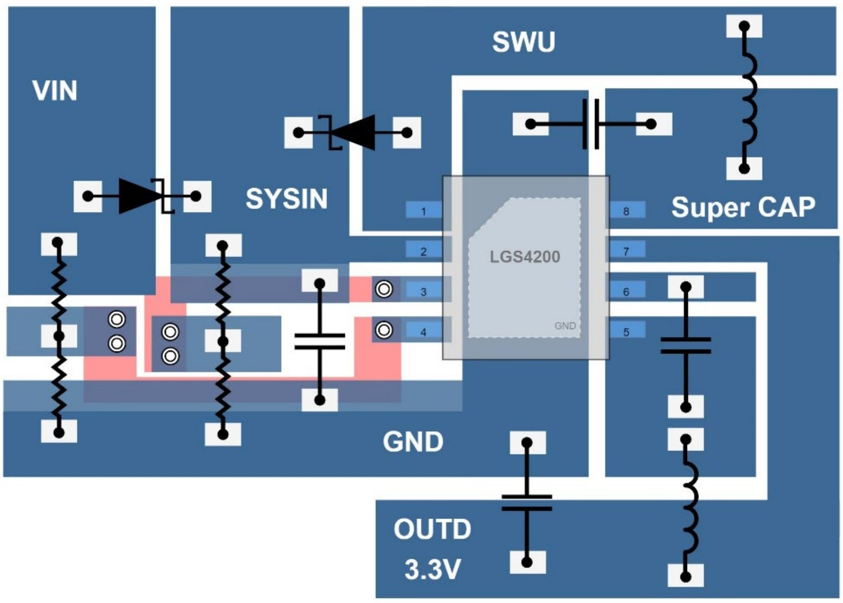
Layout

Layout Guidelines

The high integration of LGS4200 makes the PCB layout very concise and clear. Poor layout will affect the performance of LGS4200, causing electromagnetic interference (EMI), electromagnetic compatibility (EMC) poor, ground jump and voltage loss, and then affect the stability of use. In order to optimize its electrical and thermal performance, please refer to the following rules to implement PCB layout and routing to ensure the best performance:

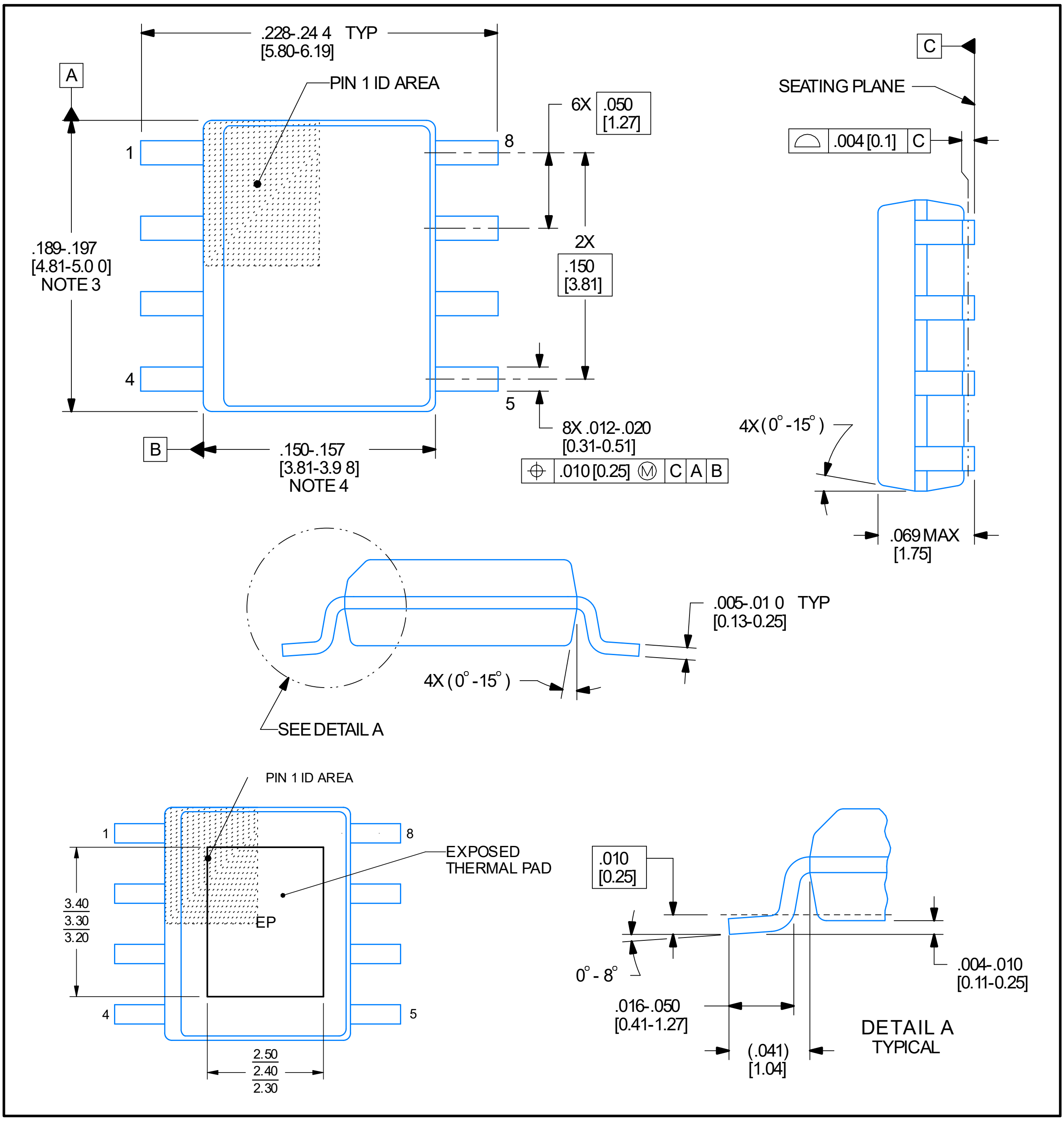
- Place the high-frequency ceramic input capacitor C_{VIN} as close as possible to the SYSIN and GND pins of LGS4200 to reduce the high-frequency noise introduced to the output pins and reduce EMI radiation. In addition, keep the input and output capacitors connected to the large area GND on the same layer.
- It is best to use a large-area copper pour method for the power circuit to make the input and output connection circuits as wide as possible, reduce the loss in the transmission process, and maximize the efficiency.
- To enhance heat dissipation and connectivity, the number of vias can be increased to realize the interconnection between the top layer and other power layers or ground layers. Please ensure that the PCB board has enough copper area for heat dissipation to keep the junction temperature below 125°C.
- The ACR and DCR losses generated by the inductance should be considered, and the heat caused by the conduction to the chip. The inductor can be placed a little further away or the heat island can be designed reasonably.
- The feedback resistors R_{FB1} and R_{FB2} should be located close to the FB pin. The feedback loop must be close to the FB and GND pins, and the distance to V_{OUTD} can be relatively farther. It is necessary to ensure that the feedback loop is far away from any noise source (such as the SW node).

Layout Example



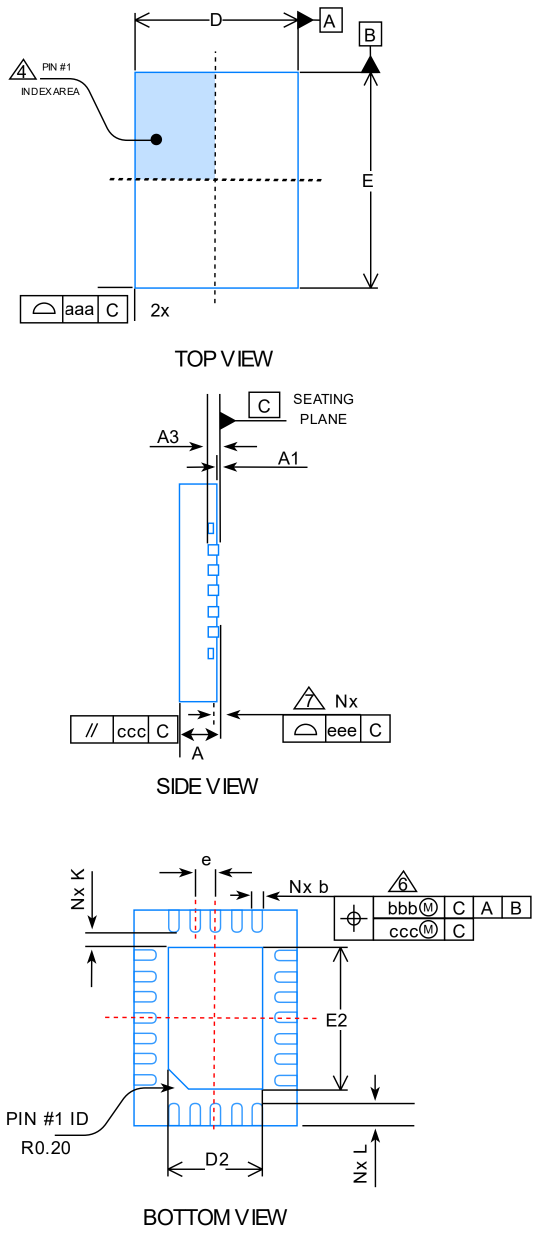
PACKAGE OUTLINE

ESOP8



PACKAGE OUTLINE

QFN3*4-24L



Dimension Table				
Symbol / Thickness	Minimum	Nominal	Maximum	NOTE
A	0.70	0.75	0.8	
A1	0.00	0.02	0.05	
A3	---	0.2Ref	---	
b	0.15	0.2	0.25	6
D	3.00 BSC			
E	4.00 BSC			
e	0.40 BSC			
D2	1.65	1.80	1.90	
E2	2.65	2.80	2.90	
K	0.15	---	---	
L	0.25	0.35	0.45	
aaa	0.05			
bbb	0.07			
ccc	0.10			
ddd	0.05			
eee	0.08			
N	24			3
ND	5			5
NE	7			5

NOTES：

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.